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REMARKS

Upon entry of this amendment, claims 1-18 and 27-34 will be pending in the above-identified application. Claims 1, 6, 8-10, 13, 15, 17, and 18 have been amended, claims 19-26 canceled, and claims 27-34 added herein. Applicant acknowledges the allowability of claim 6.

Claims 15 and 16

Claims 15 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,462,405 (Lai) in view of U.S. Patent No. 6,249,136 (Maley). As amended, claims 15 and 16 recite an electronics package disposed on the substrate, a sealant disposed on the electronics package, and an interlayer dielectric disposed between the sealant and the electronics package.

Lai discloses a semiconductor package formed by wire bonding (Fig. 1) or by a flip-chip manner using solder bumps (Fig. 2). Maley discloses an integrated circuit structure formed by C4 or flip-chip bonding using solder bumps (124) and having channels 112 formed through substrate 102. Lai and Maley, individually and in combination, fail to show or suggest an interlayer dielectric disposed between a sealant and an electronics package.

Further regarding claim 16, Lai and Maley fail to show or suggest a near-hermetic device, wherein an electronics package is solder attached to seal the package to a substrate. Lai discloses solder bumps 42 connecting chip 41 and substrate 40 but includes no indication or suggestion of a near-hermetic device having the claimed sealing characteristic.

Because Lai and Maley, individually and in combination, do not show or suggest all of the elements of claims 15 and 16, the rejection is improper. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Claims 1-4, 7, 9-14, 17, and 18

Claims 1-4, 7, 9-14, 17, and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lai in view of Maley and U.S. Patent No. 5,023,624 (Heckaman).

As amended, claims 1-4, 7, and 9-14 recite a Backside Interconnect that includes plated-through vias disposed on the MMIC and ties to terminal pins on the substrate.

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Lai discloses a semiconductor package formed by wire bonding (Fig. 1) or by a flip-chip manner using solder bumps (Fig. 2). Maley discloses an integrated circuit structure formed by C4 or flip-chip bonding using solder bumps (124) and having channels 112 formed through substrate 102. Heckaman discloses a microwave chip carrier package having a monolithic microwave integrated circuit (MMIC).

Lai, Maley, and Heckaman, separately and in combination, do not disclose or suggest a backside interconnect that includes plated-through vias disposed on the MMIC and ties to terminal pins on the substrate. In Fig. 1 of Lai, only adhesive 37 and bond wires 32 connect the chip 31 and substrate 30. Thus, if the vias 112 of Maley were added to this embodiment of Lai, they would not tie to "terminal pins on the substrate", as claimed. In Fig. 2 of Lai, solder bumps 42 connect the chip 41 to the substrate 40. If the vias 112 of Maley were added to this embodiment of Lai, they would not tie to "terminal pins on the substrate", as claimed.

Regarding claims 2-4, the cited references do not identify a substrate that is a PWB suitable for ultrahigh frequency applications, as claimed.

As amended, claim 9 further recites a plurality of rest vias connecting the MMIC to a bottom ground plane of the substrate. Maley discloses through vias 112, 228 (e.g., Figs. 7, 12, and 14). The references, individually and in combination, fail to show or suggest a plurality of rest vias connecting the MMIC to a bottom ground plane of the substrate.

As amended, claims 10 and 11 further recite a solder attachment to *near-hermetically* seal the MMIC to the substrate. The prior art fails to show or suggest the recited near-hermetic seal characteristic. Lai discloses solder bumps 42 connecting a chip 41 and a substrate 40 but contains no indication or suggestion of a near-hermetic seal, as claimed.

As amended, claims 17 and 18 recite a device having a coating and a cover disposed on the device without directly contacting the coating. Lai, Maley, and Heckaman, individually and in combination, do not show or suggest a cover disposed on the device without contacting the coating.

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As amended, claim 18 further recites that the device is substantially free of solder balls and bond pads and said coating is a low dielectric having a dielectric constant of between about 2 GHz and about 10 GHz. Lai, Maley, and Heckaman, individually and in combination, do not show or suggest these characteristics.

Because Lai, Maley, and Heckaman, individually and in combination, do not show or suggest all of the elements of claims 1-4, 7, 9-14, 17, and 18, the rejection is improper. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Claims 5 and 8

Claims 5 and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lai and Maley as applied to claim 1 and in view of U.S. Patent No. 5,396,403 (Patel). Claims 5 and 8 depend from improperly rejected claim 1.

Also, claims 5 and 8 recite a MMIC disposed on the substrate. Lai discloses a semiconductor package formed by wire bonding (Fig. 1) or by a flip-chip manner using solder bumps (Fig. 2). Maley discloses an integrated circuit structure formed by C4 or flip-chip bonding using solder bumps (124) and having channels 112 formed through substrate 102. Lai, Maley, and Patel do not show or suggest a MMIC, as claimed.

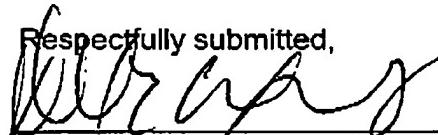
As amended, claim 8 further recites that the device is substantially free of bond wires and solder balls. Each of the cited references include bond wires and/or solder balls in their devices and does not show or suggest a device that is free of both.

Because Lai, Maley, and Patel, individually and in combination, do not show or suggest all of the elements of claims 5 and 8, the rejection is improper. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

CONCLUSION

As the application is believed to be in condition for allowance, a favorable action and a Notice of Allowance are respectfully requested.

Dated: September 13, 2004

Respectfully submitted,


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